ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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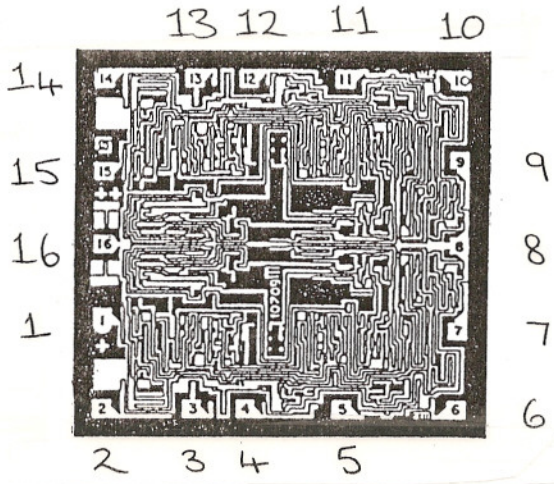
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function	Pad	Function
1	C_{X1}	9	$\overline{Q2}$
2	R_XC_X (1)	10	Q2
3	Reset (1)	11	-TR (2)
4	+TR (1)	12	+TR (2)
5	-TR (1)	13	Reset (2)
6	$\overline{Q1}$	14	R_XC_X (2)
7	Q1	15	C_{X2}
8	VSS	16	VDD

NOTE:

Pads 1, 8 and 15 are electrically connected internally.

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref: 10709B
Bond Pads (Mils): 4 X 4

APPROVED BY: **DIE SIZE (Mils): 94 X 92** **DATE: 3/13/00**
MFG: Harris **THICKNESS: 21** **P/N: CD4538BH**

DG 10.1.2
Rev A 3-4-99